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CERTIFICATE OF MAILING 37 C.F.R. § 1.8	
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:	
9/27/02 Date	<i>Ram Mitchell</i> Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:  
GEOFFREY S. STRONGIN  
DALE E. GULICK

Serial No.: 09/853,335

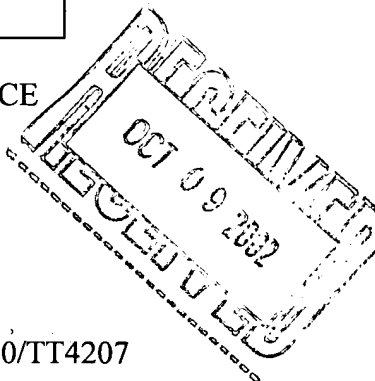
Filed: 05/11/2001

For: ASSET SHARING BETWEEN HOST  
PROCESSOR AND SECURITY  
HARDWARE

Group Art Unit: 2152

Examiner: unknown

Atty. Dkt. No.: 2000.063200/TT4207



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OCT 08 2002

INFORMATION DISCLOSURE STATEMENT

Technology Center 2100

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, it is respectfully requested that this Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

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The present Information Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Assistant Commissioner is hereby authorized to deduct said fees from Williams, Morgan & Amerson, P.C., Deposit Account No. 50-0786/2000.063200/TT4207.

This application is a continuation-in-part application of both Serial Nos. 09/852,372 and 09/853,225, both filed on May 10, 2001 and both are relied upon for an earlier filing date under 35 U.S.C. § 120. In accordance with Rule 37 C.F.R. § 1.98(d) copies of the listed documents are not enclosed as they have been previously cited by or submitted to the Patent and Trademark Office in prior application Serial Nos. 09/852,372 and 09/853,225.

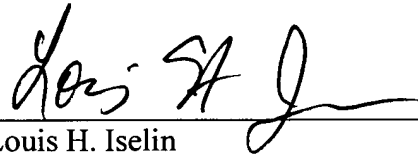
Applicant respectfully requests that the listed documents be made of record in the present case.

Applicants additional request that the following co-pending patent applications also be considered in the present case:

WMA NOS.	SERIAL NOS.
2000.038300	09/852,372
2000.038400	09/852,942
2000.038500	09/853,395
2000.038600	09/853,446
2000.038700	09/870,447
2000.038800	09/870,889
2000.038900	09/853,225
2000.039000	09/871,084
2000.039100	09/871,511
2000.039200	09/544,858
2000.039300	09/853,226
2000.039400	09/854,040

2000.039500	09/853,465	<i>Xm</i>
2000.039600	09/853,443	
2000.039700	09/853,437	
2000.080000	09/853,234	
2000.080100	09/870,890	

Respectfully submitted,



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Date: September 27, 2002

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Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

## INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.  
2000.063200/TT4207Serial No.  
09/853,335Applicant  
Strongin et al.Filing Date:  
May 11, 2001Group:  
~~2152~~ 2111U.S. Patent Documents  
*See Page 1*Foreign Patent Documents  
*See Page 1*Other Art  
*See Page 1*

## U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1						
	A2						
	A3						
	A4						
	A5						

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## Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						
	B2						
	B3						
	B4						
	B5						

## Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C1	Intel, "Low Pin Count (LPC) Interface Specification Revision 1.0," pp. 1-31 (09/29/97)
	C2	Standard Microsystems Corporation, "100 Pin Enhanced Super I/O for LPC Bus with SMBus Controller for Commercial Application," Part No. LPC47B37x, pp. 1-254 (06/17/99)
	C3	FIPS Pub 140-1 Federal Information Processing Standards Publication, "Security Requirements for Cryptographic Modules" (01/11/1994)
	C4	Intel, "Communication and Networking Riser Specification," Revision 1.0 (02/07/2000)
	C5	"Handbook of Applied Cryptography" CRC Press 1997 pp. 154 - 157, 160 - 161, 191 - 198, 203 - 212

not been considered

EXAMINER:

DATE CONSIDERED:

EXAMINER: INITIAL IF REFERENCE CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.